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Patent Number

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Attorney Docket No.: 00131-00322-US1

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Appeal Brief

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Docket No.: 00131-00322-US1
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Dennis Prather et al.

Confirmation No.: 4869

Application No.: 10/710,870

Filed: August 9, 2004

Art Unit: 2818

For: METHOD FOR CREATING FLIP-CHIP CONDUCTIVE-POLYMER BUMPS USING PHOTOLITHOGRAPHY AND POLISHING

Examiner: Calvin Lee

APPEAL BRIEF

March 27, 2006

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under § 41.37(a), this brief is timely filed within two months of the Notice of Appeal filed in this case on January 10, 2006, and is in furtherance of said Notice of Appeal.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I.	Real Party In Interest
II	Related Appeals and Interferences
III.	Status of Claims
IV.	Status of Amendments
V.	Summary of Claimed Subject Matter
VI.	Grounds of Rejection to be Reviewed on Appeal
VII.	Arguments
App. A	Claims on Appeal

App. B Evidence
App. C Related Proceedings

I. REAL PARTY IN INTEREST

Real party in interest: University of Delaware, Newark, Delaware 19716.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application: There are 10 claims pending in this application.

B. Current Status of Claims

1. Claims canceled: None
2. Claims withdrawn from consideration but not canceled: Claim 11
3. Claims pending: 1-10
4. Claims allowed: None
5. Claims rejected: 1-10

C. Claims On Appeal: The claims on appeal are claims 1-10.

IV. STATUS OF AMENDMENTS

Applicant filed a Request for Reconsideration and did not file an Amendment After Final Rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

A. Overview of Applicants' Claimed Invention

The present invention relates to semiconductor device processing, and more particularly relates to a process for creating flip-chip conductive-polymer bumps using conventional photolithography and polishing techniques. The present invention provides a low-cost and high-

resolution process that completely obviates the need for development of any dispensing/scraping equipment owing to the use of conventional micro-fabrication techniques for bump definition. This is facilitated by the use of a low-viscosity, thermoplastic conductive adhesive that is spun over lithographically patterned photoresist templates. The excess polymer material applied over the templates is removed after selective curing, by the application of a polishing step instead of using a squeegee. The use of a polishing technique offers the ability to achieve a bump surface uniformity comparable to the adhesive grain size (conducting particles are approximately 2-5 μm in diameter). This increases the effective contact area, resulting in lower contact resistance.

B. Detailed Summary of Claimed Invention with Reference to the Disclosure

A detailed discussion below is cross-referenced to the Specification and Figures as published in U.S. Patent Application Publication US 2005/0032272A1 (i.e., this application).

The present invention is a method for fabricating a flip-chip semiconductor device having plural conductive polymer bumps. In particular, the method of the present invention facilitates bump definition owing, at least in part, to the higher thermal conductivity of the under bump metallization as compared to that of a conventional methods using a photo-resist template. This higher thermal conductivity of the under bump metallization results in better adhesion of the conductive adhesive to the metal and prevents the adhesive from sticking to the photo-resist.

In addition, the method of the present invention eventually aids in stripping of the templates with high selectivity over the adhesive bumps after polishing.

Fabrication steps for an exemplary embodiment of the method of the invention are depicted in FIG. 1. In particular, **step 1** of FIG. 1 involves patterning a wafer substrate with a negative photo-resist to forming a first-level metallization. **Step 2** is a metallize and lift-off process to define the pads for the wafer substrate. Photolithography and lift-off of a negative photo-resist may be used here to pattern Titanium/Gold under bump metallization. Additional patterning is illustrated in **step 3** of FIG. 1 by providing a thick photo-resist layer to create a template greater than or equal to the desired height of the bumps. In **step 4**, the conductive

adhesive and template are baked to: (1) drive away most of the thinning solvents; and (2) make the conductive adhesive harder. The wafer may then be attached to the head of a polishing machine and the adhesive polished down to the photo-resist height in **step 5** of FIG. 1. At this point, the wafer may be inspected between repeated polishing in **step 5** to determine when polishing has removed the adhesive to the point that the surface of the photo-resist is exposed. In **step 6**, a stripper is used to remove the photo-resist molds leaving the conductive polymer bumps on the under bump metallization.

VI. GROUNDS OF OBJECTION TO BE REVIEWED ON APPEAL

A. 35 U.S.C. 103(a) rejection of claims 1-3 and 5-10 as unpatentable over US 5,587,342 (Lin et al.) in view of US 6,534,422 (Ichikawa et al.)

B. 35 U.S.C. 103(a) rejection of claim 4 as unpatentable over Lin et al. in view of Ichikawa et al. as applied to claim 1, and further in view of US Patent Application No. US2005/0025973 (Slutz et al.)

VII. ARGUMENT

Legal Principles

To establish a *prima facie* case of obviousness, three basic criteria must be met: (1) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; (2) there must be a reasonable expectation of success; and (3) the prior art reference must teach or suggest all the claim limitations.[1] Further, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not just within the applicant's disclosure.[2]

[1] *See* MPEP §2143.
[2] *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) and *See* MPEP §2143.

Combining prior art references without evidence of a suggestion, teaching or motivation simply takes the inventors' disclosure as a blueprint for piecing together the prior art to defeat patentability – the essence of hindsight.[3]

"There are three possible sources for a motivation to combine references: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art."[4] Further with regard to the level of skill of practitioners in the art, there is nothing in the statutes or the case law which makes "that which is within the capabilities of one skilled in the art" synonymous with obviousness.[5] The level of skill in the art cannot be relied upon to provide the suggestion to combine references.[6]

In accordance with the above-discussed legal principles, this Brief responds to the rejections of the claims on appeal as set forth in the explicit statements of the rejections. In particular, claims 1-3 and 5-10 were rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Ichikawa et al. Applicants respectfully traverse the rejection.

1. The 35 U.S.C. 103(a) obviousness rejection over Lin et al. in view of Ichikawa et al. is deficient, as the applied art does not teach or suggest all the limitations of claims 1-3 and 5-10.

-Discussion of the deficiencies of Lin et al.

Lin et al. discloses a method for forming an electrical interconnect that includes interconnecting bumps that are formed on a circuit substrate using printing or dispensing techniques with a wet photoresist layer as a mask.[7] In particular, Lin et al. discloses a method comprising the steps of: providing a substrate; forming a conductive layer on a portion of the substrate; forming a wet photoresist layer on the substrate and the conductive layer; patterning the wet photoresist layer to form openings to the conductive layer; disposing a conductive paste in at least the openings to the conductive layer; heating the conductive paste a first time at a

[3] *Interconnect Planning Corp. v. Feil*, 227 USPQ 543 (Fed. Cir. 1985)
[4] *See* MPEP §2143.01, citing *In re Rouffet*, 149 F.3d, 1350, 1357, 47 USPQ2d 1453, 1457-8 (Fed. Cir. 1998).
[5] *Ex parte Gerlach and Woerner*, 212 USPQ 471 (PTO Bd. App. 1980).
[6] *See* MPEP §2143.01, citing *Al-Site Corp. v. VSI Int'l Inc.*, 50 USPQ2d 1161 (Fed. Cir. 1999).
[7] Lin et al. at ABSTRACT.

temperature above room temperature; removing the wet photoresist layer; and heating the conductive paste at a temperature above room temperature a second time after the step of removing the wet photoresist layer.[8]

More specifically, Lin et al. discloses *sweeping* **42** the conductive paste **30** with a squeegee **40** across the wet photoresist layer **15**, forcing the conductive paste **30** into openings **20** and removing the excess conductive paste **30** off of photoresist mask **15**; or *applying pressure* to the conductive paste **30** through any means, such as a disk **50**, that forces conductive paste **30** into openings **20** and removing the excess conductive paste **30** off of photoresist mask **15** (emphasis added).[9]

However, Lin et al. nowhere discloses, as recited in claim 1:

> *polishing* the conductive polymer layer to remove excess conductive polymer material from a surface of the photoresist (emphasis added).

That is, as discussed above, Lin et al. discloses either *sweeping* **42** the conductive paste **30** with a *squeegee* **40** or *applying pressure* to the conductive paste **30** "to remove excess conductive paste **30**."[10] In contrast to Lin et al., claim 1 recites the limitation of "*polishing* the conductive polymer layer to remove excess conductive material" (emphasis added).

In addition, paragraph 4, lines 1-6 of the outstanding Office Action indicates the statement in Lin et al. that "the surface of the conductive paste **30** is *planer* ... having substantially the same height" *inherently teaches* the step of polishing the conductive polymer layer (emphasis added). Applicants respectfully disagree.

Applicants respectfully point out that the Manual of Patent Examining and Procedure (MPEP) Section 2112 (IV) requires that the:

> **EXAMINER MUST PROVIDE RATIONALE OR EVIDENCE TENDING TO SHOW INHERENCY.**

In particular, MPEP Section 2112 (IV) states:

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[8] *Id.* at FIG. 1 – FIG. 7, column 6, lines 6-23.
[9] *Id.* at FIG. 3 – FIG. 4, column 3, lines 39-67.
[10] *Id.* at FIG. 3 and FIG. 4; column 3, lines 39-60;

> [t]he fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic.[11]

More specifically, MPEP Section 2112 (IV) states:

> [i]n relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art.[12]

Thus, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art. It was requested that the Examiner provide this information before making the outstanding Office Action final.

In contrast to the allegation of inherency in the outstanding Office Action, it is respectfully submitted that the allegedly inherent characteristic does not necessarily flow from the teachings of Lin et al. In particular, Applicants submit that the surface of the conductive paste being "planer," as recited in Lin et al., clearly does *not inherently teach* the limitation of "polishing," as recited in claims 1 and 10. To emphatically prove this point, one need only reference the words of Lin et al. cited in the outstanding Office Action in context. In particular, the entire statement from Lin et al. is as follows:

> [i]n a preferred embodiment, *conductive paste **30** fills opening **20** so that the surface of conductive paste **30** is planer* with wet photoresist layer **15** in order to provide interconnect bumps having substantially the same height (emphasis added).[13]

The specifics of how the conductive paste **30** is made to fill the openings **20** so that "the surface of the conductive paste **30** is planer" is provided by further examining the context in which Lin et al. makes the above statement. In particular, Lin et al. discloses:

> *a squeegee* **40** or other suitable instrument is used to *sweep* conductive paste **30** across wet photoresist layer **15** thereby *forcing conductive paste **30** into openings **20*** and removing the excess conductive paste **30** off of photoresist mask **15**. *It is necessary to substantially fill openings **20*** and to substantially remove excess

[11] *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993).
[12] *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990).
[13] *See* Lin et al. at column 4, lines 12-16.

> conductive paste **30** from the surface of wet photoresist layer **15** (emphasis added).[14]

That is, Lin et al. explicitly teaches, "*a squeegee* **40** or other suitable instrument is used to *sweep* conductive paste **30** across wet photoresist layer **15** for the purpose of *forcing conductive paste 30 into openings 20*, and not for the purpose of "polishing the conductive polymer layer," as recited in claim 1 and claim 10. Moreover, Lin et al. discloses that the step of "forcing conductive paste" into openings **20** with the squeegee is "necessary" and "fills the openings **20** *so that the surface of conductive paste 30 is planer*."

Thus, it is respectfully submitted that the above discussion indicates that the statement, which was referenced in the outstanding Office Action, as inherently teaching "polishing" due to the use of the term "planer," clearly does *not* explicitly nor inherently teach or suggest the step of "polishing" as recited in the claims 1 and 10 of the invention.

Furthermore, the specification of the invention *explicitly teaches away from the use of "squeegee-based" or "pressure-based" approaches* and includes test results emphasizing the benefits of "polishing," as recited in claims 1 and 10.[15] In particular, the specification teaches the application of "a polishing step instead of using a squeegee."[16] Further, the specification teaches and the test results indicate that better surface uniformity is obtained by "polishing as compared to squeegee."[17]

Thus, Lin et al. not only does not disclose the claimed invention but it in fact *teaches away* from the claimed invention by disclosing the use of "squeegee-based" or "pressure-based" approaches. Therefore, it is respectfully submitted that Lin et al. does not disclose, suggest or make obvious the claimed invention and that claim 1 and claim 10, and claims dependent thereon, patentably distinguish thereover.

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[14] *Id.* at column 3, lines 40-47.
[15] Specification at paragraphs 15 and 51-55 of published US Application no. US2005/0032272A1.
[16] *Id.* at paragraph 15, lines 6-11.
[17] *Id.* at paragraph 55, lines 8-10.

Furthermore, the outstanding Office Action acknowledges other deficiencies of Lin et al. and attempts to overcome these deficiencies by combining Lin et al. with Ichikawa et al.[18] However, Ichikawa et al. cannot overcome all of the deficiencies of Lin et al., *as discussed above*, with regards to the claimed invention.

-Discussion of the deficiencies of Ichikawa et al.

Ichikawa et al. discloses an Electro-Static Discharge (ESD) structure that is created on an integrated circuit by providing a conductive polymer material between a signal line and a supply node or ground reference.[19] In addition, Ichikawa et al. discloses that the conductive polymer material becomes conductive when an electric field of sufficient intensity is applied.[20]

However, Ichikawa et al. nowhere discloses, as recited in claim 1:

> *polishing* the conductive polymer layer to remove excess conductive polymer material from a surface of the photoresist (emphasis added).

That is, in contrast to Ichikawa et al., claim 1 and claim 10 recite the limitation of "polishing the conductive polymer layer to remove excess conductive material." In addition, a word search of Ichikawa et al. nowhere reveals either the term "polish" or "polishing." *Since nothing in Ichikawa et al. has been cited that discloses this limitation,* Ichikawa et al. cannot overcome all of the deficiencies of Lin et al.

Therefore, it is respectfully submitted that neither Lin et al. nor Ichikawa et al., whether taken alone or in combination, disclose, suggest or make obvious the claimed invention and that claim 1, claim 10 and claims dependent thereon, patentably distinguish thereover.

Claim 4 was rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Ichikawa et al., as applied in claim 1, and further in view of Slutz et al. Applicants respectfully traverse the rejection.

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[18] Outstanding Office Action, page 2, paragraph 3f.
[19] Ichikawa et al. at ABSTRACT.
[20] *Id.*

2. The 35 U.S.C. 103(a) obviousness rejection over Lin et al. in view of Ichikawa et al., as applied in claim 1, and further in view of Slutz et al. is deficient, as the applied art does not teach or suggest all the limitations of claim 4.

-Discussion of the deficiencies of Lin et al. and Ichikawa et al.

Claim 4 ultimately depends upon claim 1. As discussed above, neither Lin et al. nor Ichikawa et al., whether taken alone or in combination, disclose the limitations of claim 1. Thus, at least for the reasons discussed above, neither Lin et al. nor Ichikawa et al., whether taken alone or in combination, disclose the limitations of claim 4.

In addition, the outstanding Office Action acknowledges other deficiencies of Lin et al. and Ichikawa et al. and attempts to overcome these deficiencies by combining Lin et al. and Ichikawa et al. with Slutz et al.[21] However, Slutz et al. cannot overcome the deficiencies of Lin et al. and Ichikawa et al., *as discussed above*, with regards to the claimed invention as will be discussed below.

-Discussion of the deficiencies of Slutz et al.

Slutz et al. discloses a composite material and the method of making same, which comprises a CVD diamond coating applied to a composite substrate of ceramic material and an unreacted carbide-forming material of various configurations and for a variety of applications.[22]

However, Slutz et al. nowhere discloses, as recited in claim 1 and claim 4:

> *polishing* the conductive polymer layer to remove excess conductive polymer material from a surface of the photoresist (emphasis added).

That is, in contrast to Slutz et al., claim 1 and claim 4 both recite the limitation of "polishing the conductive polymer layer to remove excess conductive material." *Since nothing in Slutz et al. has been cited that discloses this limitation,* Slutz et al. cannot overcome the deficiencies of Lin et al. and Ichikawa et al.

[21] Outstanding Office Action, page 2, paragraph 4.
[22] Slutz et al. at ABSTRACT.

Therefore, it is respectfully submitted that none of Lin et al., Ichikawa et al. or Slutz et al., whether taken alone or in combination, disclose the claimed invention and that claim 1, claim 4 and claims dependent thereon, patentably distinguish thereover.

3. The outstanding Advisory Action misrepresents the applicability of Admitted Prior Art to the present invention.

The Advisory Action states:

> such polishing of a polymer is known in the semiconductor processing art as evidenced by Applicant's Prior Art disclosing, ". . . scraping and dispensing the polymer material by use of a polishing technique" [paragraph 10].[23]

However, the prior art reference cited in the Advisory Action and the specification is actually directed at polishing a "high velocity polymer. In contrast, the claimed invention is facilitated by "applying a low-viscosity conductive polymer material," as recited in claim 1. Therefore, the prior art discussion in the specification is not applicable to the present invention.

VIII. CLAIMS

A copy of claims 1-10 involved in the present appeal is attached hereto as Appendix A.

[23] Advisory Action at page 2.

Application No.: 10/710,870 Docket No.: 00131-00322-US1

In view of the Arguments presented above, reversal of the rejections by the Honorable Board and allowance of pending claims 1-10 is respectfully requested.

Date: March 27, 2006

Respectfully submitted,

By Myron Keith Wyche
Myron Keith Wyche
Registration No.: 47,341
CONNOLLY BOVE LODGE & HUTZ LLP
Agent for Applicant

APPENDIX A- CLAIMS ON APPEAL

Claims Involved in the Appeal of Application Serial No. 10/710,870

LISTING OF CLAIMS

1. (Original) A method for fabricating a flip-chip semiconductor device having plural conductive polymer bumps thereon, the method comprising:

patterning and depositing metallized pads on a substrate;

photolithographically forming plural molds on the substrate using a photoresist, wherein the plural molds are in registration with the metallized pads;

filling each of the plural molds by applying a low-viscosity conductive polymer material; spinning the substrate to form a uniformly distributed conductive polymer layer;

baking the substrate, plural molds, and conductive polymer material to thicken any remaining conductive polymer material and evaporate any solvent in the conductive polymer layer;

polishing the conductive polymer layer to remove excess conductive polymer material from a surface of the photoresist;

stripping the plural molds to reveal the plural conductive polymer bumps; and

hardening the plural conductive polymer bumps by temperature curing.

2. (Original) The method of claim 1, wherein the photoresist is a negative resist.

3. (Original) The method of claim 1, wherein the photoresist is a positive resist.

4. (Original) The method of claim 1, further comprising, after polishing the conductive polymer layer, fine polishing the conductive polymer layer using a grid having a grain size smaller than a first grain size used in polishing the conductive polymer layer.

5. (Original) The method of claim 1, wherein baking the substrate is accomplished at a temperature in a range of approximately 70C-120C.

6. (Original) The method of claim 1, wherein stripping the plural molds is accomplished using a resist remover.

7. (Original) The method of claim 1, wherein the temperature curing is accomplished at a temperature in the range of approximately 190C-230C.

8. (Original) The method of claim 1, wherein the temperature curing is accomplished at a temperature of approximately 190C for about 30 minutes.

9. (Original) The method of claim 1, wherein the temperature curing is accomplished at a temperature equal to or greater than a glass transition temperature of the conductive polymer.

10. (Original) A method for fabricating a flip-chip semiconductor device having high aspect ratio plural conductive polymer bumps thereon, the method comprising: forming plural molds on a substrate using a photolithographic technique; filling the molds by spinning a layer of conductive polymer material onto the substrate; polishing the conductive polymer material layer to remove excess conductive material from a surface of the substrate; and exposing the plural conductive polymer bumps by removing the plural molds from the substrate.

11. (Withdrawn) An integrated semiconductor package produced by the method of any one of claims 1-10, the package comprising a plurality of conductive polymer bumps electrically connected to respective under bump metallization contacts, wherein the under bump metallization contacts are operatively connected to a semiconductor device.

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APPENDIX B – EVIDENCE

NONE

APPENDIX C - RELATED PROCEEDINGS

NONE